Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor construction assembly including: (i) a semiconductor substrate having first and second surfaces that are mutually opposed to each other, and a plurality of side surfaces between the first surface and the second surface,(ii) an integrated circuit element formed on the first surface, (iii) a plurality of connection pads which are arranged on the first surface and connected to the integrated circuit element, (iv) a protective layer which is formed to cover the first surface of the semiconductor substrate and which has openings for exposing the connection pads, (v) a plurality of conductors which are connected to the connection pads and arranged on the protective layer and which have pads, (vi) columnar electrodes formed on the pads of the conductors, and (vii) a sealing film formed between the columnar electrodes and on the protective layer;

a sealing member which covers at least one side surface of the semiconductor construction assembly;

an upper insulating layer which covers the semiconductor construction assembly and the sealing member except for portions corresponding to the columnar electrodes so as to expose an upper surface of each of the columnar electrodes;

upper conductors which are formed on the upper insulating layer, and each of which includes one end that is electrically connected to the pad of one of the conductors via one of the columnar electrodes and at least one external connection pad;

wherein an external connection pad of at least one of the upper conductors is disposed in a region opposing the sealing member; and

wherein an additional insulating layer made of an inorganic material is formed between the semiconductor substrate and the protective layer of the semiconductor construction assembly.

Claims 2 and 3 (Canceled).

4. (Previously Presented) A semiconductor device according to claim 1, wherein upper surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

5. (Previously Presented) A semiconductor device according to claim 1, wherein lower surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

Claims 6 and 7 (Canceled).

8. (Original) A semiconductor device according to claim 1, further comprising a base member which holds the semiconductor construction assembly and the sealing member.

Claims 9 and 10 (Canceled).

11. (Currently Amended) A semiconductor device ~~according to claim 1,~~ comprising:

a semiconductor construction assembly including: (i) a semiconductor substrate having first and second surfaces that are mutually opposed to each other, and a plurality of side surfaces between the first surface and the second surface,(ii) an integrated circuit element formed on the first surface, (iii) a plurality of connection pads which are arranged on the first surface and connected to the integrated circuit element, (iv) a protective layer which is formed to cover the first surface of the semiconductor substrate and which has openings for exposing the connection pads, (v) a plurality of conductors which are connected to the connection pads and arranged on the protective layer and which have pads, (vi) columnar electrodes formed on the pads of the conductors, and (vii) a sealing film formed between the columnar electrodes and on the protective layer;

a sealing member which covers at least one side surface of the semiconductor construction assembly;

an upper insulating layer which covers the semiconductor construction assembly and the sealing member except for portions

corresponding to the columnar electrodes so as to expose an upper surface of each of the columnar electrodes;

upper conductors which are formed on the upper insulating layer, and each of which includes one end that is electrically connected to the pad of one of the conductors via one of the columnar electrodes and at least one external connection pad;

wherein an external connection pad of at least one of the upper conductors is disposed in a region opposing the sealing member; and

wherein the sealing member comprises a buried member, and the buried member has substantially a same thickness as a thickness of the semiconductor construction assembly.

Claim 12 (Canceled).

13. (Previously Presented) A semiconductor device according to claim 11, wherein a further insulating material is filled between the buried member and the semiconductor construction assembly.

14. (Currently Amended) A semiconductor device ~~according to claim 1,~~ comprising:

a semiconductor construction assembly including: (i) a semiconductor substrate having first and second surfaces that are mutually opposed to each other, and a plurality of side surfaces

between the first surface and the second surface, (ii) an integrated circuit element formed on the first surface, (iii) a plurality of connection pads which are arranged on the first surface and connected to the integrated circuit element, (iv) a protective layer which is formed to cover the first surface of the semiconductor substrate and which has openings for exposing the connection pads, (v) a plurality of conductors which are connected to the connection pads and arranged on the protective layer and which have pads, (vi) columnar electrodes formed on the pads of the conductors, and (vii) a sealing film formed between the columnar electrodes and on the protective layer;

a sealing member which covers at least one side surface of the semiconductor construction assembly;

an upper insulating layer which covers the semiconductor construction assembly and the sealing member except for portions corresponding to the columnar electrodes so as to expose an upper surface of each of the columnar electrodes;

upper conductors which are formed on the upper insulating layer, and each of which includes one end that is electrically connected to the pad of one of the conductors via one of the columnar electrodes and at least one external connection pad;

wherein an external connection pad of at least one of the upper conductors is disposed in a region opposing the sealing member; and

wherein interlayer conductors which connect the conductors of the semiconductor construction assembly and the upper conductors, and an interlayer dielectric layer which covers the interlayer conductors are arranged between the upper conductors and the semiconductor construction assembly.

15. (Previously Presented) A semiconductor device according to claim 14, wherein an uppermost insulating layer is arranged on an upper surface of the interlayer dielectric layer and on the upper conductors and does not cover the external connection pads of the upper conductors.

16. (Previously Presented) A semiconductor device according to claim 15, further comprising projecting connection terminals arranged on the external connection pads of the upper conductors.

17. (Previously Presented) A semiconductor device according to claim 16, wherein each of the projecting connection terminals comprises a solder ball.

18. (Withdrawn) A semiconductor device according to claim 15, wherein at least one electronic component which is electrically connected to at least one of the external connection pads is arranged on the uppermost insulating layer.

19. (Withdrawn) A semiconductor device according to claim 15, wherein at least one connection pin is arranged on at least one of the external connection pads.

20. (Withdrawn) A semiconductor device according to claim 1, further comprising at least one electrical connection member which is electrically connected to at least one of the upper conductors, and which extends vertically through the sealing member from an upper surface of the sealing member to a lower surface of the sealing member.

Claims 21-40 (Canceled).

41. (New) A semiconductor device comprising:

a semiconductor construction assembly including: (i) a semiconductor substrate having first and second surfaces that are mutually opposed to each other, and a plurality of side surfaces between the first surface and the second surface,(ii) an integrated circuit element formed on the first surface, (iii) a plurality of connection pads which are arranged on the first surface and connected to the integrated circuit element, (iv) a protective layer which is formed to cover the first surface of the semiconductor substrate and which has openings for exposing the connection pads, (v) a plurality of conductors which are connected to the connection pads and arranged on the protective

layer and which have pads, (vi) columnar electrodes formed on the pads of the conductors, and (vii) a sealing film formed between the columnar electrodes and on the protective layer;

a sealing member which covers at least one side surface of the semiconductor construction assembly;

an upper insulating layer which covers the semiconductor construction assembly and the sealing member except for portions corresponding to the columnar electrodes so as to expose an upper surface of each of the columnar electrodes;

upper conductors which are formed on the upper insulating layer, and each of which includes one end that is electrically connected to the pad of one of the conductors via one of the columnar electrodes and at least one external connection pad;

wherein an external connection pad of at least one of the upper conductors is disposed in a region opposing the sealing member; and

wherein upper surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

42. (New) A semiconductor device according to claim 41, wherein lower surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

43. (New) A semiconductor device according to claim 41, further comprising a base member which holds the semiconductor construction assembly and the sealing member.

44. (New) A semiconductor device according to claim 11, wherein an additional insulating layer made of an inorganic material is formed between the semiconductor substrate and the protective layer of the semiconductor construction assembly.

45. (New) A semiconductor device according to claim 11, wherein upper surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

46. (New) A semiconductor device according to claim 11, wherein lower surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

47. (New) A semiconductor device according to claim 11, further comprising a base member which holds the semiconductor construction assembly and the sealing member.

48. (New) A semiconductor device according to claim 14, wherein an additional insulating layer made of an inorganic material is formed between the semiconductor substrate and the protective layer of the semiconductor construction assembly.

49. (New) A semiconductor device according to claim 14, wherein upper surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

50. (New) A semiconductor device according to claim 14, wherein lower surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

51. (New) A semiconductor device according to claim 14, further comprising a base member which holds the semiconductor construction assembly and the sealing member.